Amendments to the Specification:

In the SUMMARY OF THE INVENTION,
please replace 3 paragraphs starting at the the 4th paragraph beginning up to the last paragraph on page 5 with the following 3 amended paragraphs:

In the same way aAs described in the referenced patent application (US Serial No. 10/764920), within a set of small capacitors, one capacitor after the other is switched in parallel to change the total sum of capacitance. To achieve a linear capacitance change, said capacitors are not switched on one by one in digital steps, however each capacitor is switched on partially in a sliding operation, starting at low value (0 % of its capacitance) and ending with the fully switched on capacitor (100 % of its capacitance). To achieve said sliding switch operation, a typical implementation uses FET- type transistors as switching device, one per capacitor. The switching operation of such FET-type transistor can be divided into three phases: the fully-switched-off phase (said FET transistor's drain-source-resistance RDS is very high), a steady ramp-up/ramp-down phase or steady transition phase (that is: said FET transistor's resistance RDS is changing between very high resistance and very low resistance in a linear and steady mode) and the fully-switched-on phase (said FET transistor's drain-source-resistance RDS is very low). By thoroughly controlling such switching device within said linear and steady ramp-up/ramp-down phase, the capacitor in series with said switching device is partially switched in parallel with a well-controlled proportion between 0 % and 100 %.

The terms "steady ramp-up/ramp-down phase" or "steady transition phase" (and "steady ramp-up/ramp-down area" or "steady transition area") are used as synonyms throughout this document. The term "area" in this context is used to express the "operating range" – the term "phase" is used to express the "operation in process" within said area.

One key point to obtain highest possible Q-factor is to have at any time only one (or very few) transistor in the steady transition phase, i.e. RDS~~on–~~ changeing -mode; all other transistors are either fully switched on or fully switched off. To achieve this goal, an individual threshold level for each capacitor switching stage defines the point where, in relation to the tuning voltage, each of said capacitor switching stages switches from the off to the on state. Overlapping of neighboring switching stages cannot be completely eliminated, but overlapping is kept to a minimum by selecting appropriate threshold parameters.

Please replace all paragraphs, starting at the 2nd full paragraph at page 6 up to the 2nd full paragraph on page 8 with the following amended paragraphs:

While the switching transistor is kept within its steady transition phase (RDS steady changing mode) the resistance of ~~the~~ said switching transistor linearly follows the input difference of said translinear amplifier. As said translinear amplifier can

operate at different absolute voltage levels at their input and output, the resulting level shifting operation is best suitable for said switching transistor's operation.

Additional circuit elements, described in the related US Patent Application, Serial No. 10/676919, filed Oct. 1, 2003, titled "Translinear Amplifier" and hereby incorporated by reference, implement a signal~~-limiting~~ cutoff function ~~and~~ by ~~provide~~ providing a signal to sharply cut off said translinear amplifier's linear operation, once the defined linear operating range is exceeded at the negative end of said linear operating range; and to sharply limit said translinear amplifier's linear operation, once the linear operating range is exceeded at the positive end of said linear operating range. The circuits of said signal~~-limiting~~ cutoff functions then either overdrive said switching transistor either into deep saturation (RDSon going to 0) or overdrive it into its extreme off state (RDSoff going very high) when said switching device ~~is~~ operates outside its desired steady transition phase.

There are various techniques to generate a set of reference values defining the threshold ~~points~~ levels for the input and output references levels of each of said translinear amplifier stages. And there are various techniques to provide a tuning voltage, dedicated for the voltage controlled capacitance change, to all of said amplifier stages.

The total concept according to the proposed invention is shown in **Fig. 6**. One key point of the invention is the implementation of signal~~-limiting~~ cutoff functions at both ends of the steady ramp-up/ramp-down phase. Once the signal controlling the switching device leaves the steady transition phase, the signal condition is changed abrupt. **Fig. 7** visualizes this effect. The purpose is to overdrive said switching device to a fully-on state, when said switching device ~~is~~ operates outside its steady transition ~~phase~~ area on the low~~er~~ resistance side (low RDSon) and to overdrive said switching device to a fully-off status, when said switching device ~~is beyond~~ leaves its steady transition ~~phase~~ area on the high~~er~~ resistance side (high RDSo~~n~~ff).

Depending on the technique to implement the reference values for each of the translinear amplifiers within a chain of said ~~translinear amplifiers~~ capacitor switching stages, even specific nonlinear relations of capacitance change versus tuning voltage can be constructed.

In accordance with the objectives of this invention, a set of individual capacitors is implemented. Such capacitors could, for example, be discrete metal or polymer capacitors on a common planar carrier or they could be integrated on a semiconductor substrate. The switching device is typically a FET transistor, which could be for example a P-~~MOS~~channel or N-~~MOS~~-channel junction FET or a ~~C~~PMOS or NMOS FET.

The amplifier primarily generating the control signal for the switching devices is, according to the invention, a translinear amplifier, as described in patent application, US Serial No. 10/676919, filed Oct. 1, 2003. In addition, signal~~-limiting~~ cutoff functions, which are designed to drive said switching device to a fully-on status, when said

switching device ~~is~~ operates outside its steady transition ~~phase~~ area on the low~~er~~ resistance side (low RDSon) or to drive said switching device to a fully-off status, when said switching device ~~is~~ operates outside its steady transition ~~phase~~ area on the high~~er~~ resistance side (high RDSo~~n~~ff), can be implemented. Such signal ~~limiting~~ cutoff functions could, according to the invention, be implemented with additional circuit elements within the translinear amplifier. They could however be implemented as separate circuits as well.

The circuit also provides the components to generate the set of reference voltages for the threshold ~~voltages~~ levels of each ~~amplifier~~ capacitor switching stage. A resistor chain is one possible solution. The amplifiers within each capacitor switching stage then use the tuning voltage supplied and said reference voltages to generate the control signal for said switching devices, which then switch the capacitors in parallel, one after the other.

Please replace the first three paragraphs on page 9 and continuing into page 10 with the following three amended paragraphs:

Even further, a specific non-linear characteristic of the tuning voltage to capacitance relation can be achieved by dimensioning the relation between said tuning voltage and said individual threshold ~~points~~ levels as desired. In one proposed solution, the individual steps of the reference resistor chain will be dimensioned to ~~the~~ a desired nonlinear curve, for example when the steps between the threshold ~~points~~levels, where the next capacitor starts to be switched on, are narrower in one area than in other areas, more capacitors start to be switched in parallel and a steeper change of total capacitance can be achieved. .

A translinear amplifier typically has a gain of 1. However, a gain different from 1 is also achievable, which, if implemented, gives one more degree of freedom in dimensioning and optimizing certain operating parameters. For example, the remaining overlapping of neighboring capacitor switching stages may be even further reduced, as the ~~slope~~ steepness of the steady ramp-up/ramp-down operation can be controlled with adequate selection of the gain.

In accordance with the objectives of this invention, a method to control the capacitance of a variable capacitor in a strictly linear mode through a tuning voltage and to achieve a high Q-factor at the same time generate, is achieved. One method is to switch a variable number of capacitors in parallel, where only one is in the steady transition phase of being switched on (or off) in a steady progressing mode (i.e. the effective capacitance being ramped-up or ramped-down). All other capacitors of a larger number of capacitors are either already fully switched on or are still complete switched off. One key method is to linearly control the switching function for each of said switching devices, when said switching device is in an analog mode within the steady transition phase but to change the signal abrupt, as soon as the control signal for said switching function leaves its steady transition area. One method drives said switching device to a fully-on status, when said switching device ~~is~~ operates outside its

steady transition area on the lowe~~r~~ resistance side. A similar method drives said switching device to a fully-off status, when said switching device is beyond its steady transition area on the highe~~r~~ resistance side. A further method amplifies, by a translinear amplifier, the difference of the capacitance tuning voltage and the reference voltage of each amplifier stage, producing the linear control signal for said steady progressing switching operation. Another method generates a set of reference values, one for each of said amplifier stages. Finally, the circuit supplies a tuning voltage, dedicated for the voltage controlled capacitance change, to all of said amplifier stages.

Please replace the first paragraph on page 11 with the following amended paragraph:

An even further method is to produce threshold ~~points~~ <u>levels</u> ~~(or reference points)~~ along a non-linear curve<u>, i.e. by not spreading the threshold points with equal distances</u> ~~and~~ <u>in order to</u> get~~ting~~ a desired non-linear relation of the total capacitance change~~s~~ versus tuning voltage.

In the BRIEF DESCRIPTION OF THE DRAWINGS.,
please replace the description of Fig. 4a with the following amended description:

Fig. 4a shows the gate voltage versus tuning voltage relation for the ~~series~~ <u>chain</u> of capacitor switching stages, according to Fig. 3.

Please add the description for Fig. 4c as follows:

<u>**Fig. 4c** visualizes the reduced signal overlapping effect of 2 adjacent stages with steeper control signals.</u>

Please replace the description of Fig. 6 with the following amended description:

Fig. 6 shows the circuit schematic of multiple capacitor switching stages<u>,</u> <u>each</u> ~~with~~ <u>comprising</u> a ~~chain of~~ translinear amplifier~~s~~, in accordance with an embodiment of this invention.

Please add the description for Fig. 10a as follows:

<u>**Fig. 10a** shows the additional circuits to provide the cutoff signals to overdrive the switching devices to a fully off or fully on state.</u>

Please change the number of previous Fig. 10 to Fig. 10b as follows:

Fig. 10b shows the added circuit to generate a temperature compensated reference voltage.

In the DESCRIPTION OF THE PREFERRED EMBODIMENTS, please replace the 3rd paragraph at page 14 with the following amended paragraph:

Fig. 3 shows a principal circuit diagram of the referenced related patent application. A set of circuits to control the switching operation in a ramp-up/ramp-down manner, contains, typically besides other components, the set of operational amplifiers **Amp 1** to **Amp n**. **Sw 1** to **Sw n** are said switching devices and **Cap 1** to **Cap n** are said capacitors that will be switched in parallel. As an example, a resistor chain **R1** to **Rn**, or a similar circuit, produces a series of voltage references **Ref 1** to **Ref n** and each of said operational amplifiers compares the tuning voltage input with its dedicated reference voltage. The resulting variable capacitance is available at the output ~~points~~ connector **varCap**. As a minimum circuit implementation, a simple wire connection feeds the tuning voltage directly to the amplifier inputs.

Please add the following paragraph after the 3rd paragraph on page 14:

The herewith disclosed invention replaces said operational amplifiers of the referenced related patent application Serial No. 10/764920 with translinear amplifiers, as shown in **Fig. 6**.

Please move three paragraphs starting with the 2nd full paragraph on page 18 forward to a position just after the above (new) 4th paragraph on page 14 and delete them from the original position. These 3 paragraphs are further amended to the following:

According to the objectives of this invention, the operational amplifiers, within said set of circuits to control the switching operation in a ramp-up/ramp-down manner, as shown in **Fig. 3**, are replaced by translinear amplifiers. A single stage of said capacitor switching function is presented in **Fig. 5** and the total circuit schematic for multiple stages according to the proposed invention is shown in **Fig. 6**, where a set of circuits to control the switching operation in a ramp-up/ramp-down manner, contains, typically besides other components, the set of translinear amplifiers. Key advantage is the fact, that the voltage levels at the translinear amplifier inputs and at the translinear amplifier outputs are independent, only the differential voltage at the inputs and at the outputs is important. Said translinear amplifier works in this context as a level shifter. Such translinear amplifiers have typically a gain of 1.

The translinear amplifier in **Fig. 5** compares the differential voltage at its inputs **Vinp-5** and **Vinn-5** and, through various current mirroring techniques, provides the same differential voltage at its outputs **Voutp-5** and **Voutn-5**; i.e. the output difference of said amplifier strictly follows the difference at said amplifier inputs, independent of the absolute voltage level at the outputs. The translinear amplifier then drives said current switching device **N1-5** with the gate voltage **Vg-5** to switch on said individual small capacitor **Cap-5** in the proposed steady ramp-up/ramp-down manner.

Each of said translinear amplifiers can operate at a different absolute voltage level at their input and work independent at another output level. In this way the network to generate the reference voltages can be optimized independently for each stage, because the voltage level best suitable for the control operation of each switching transistor can be freely selected. In the circuit shown in **Fig. 6** as an example, the reference voltages are produced in a simple chain of resistors. The translinear amplifiers **Tr.Amp 1** to **Tr.Amp n** can adjust between said input reference voltage levels **Ref-in 1** to **Ref-in n** and the output reference levels **Ref-out-1** to **Ref-out-n**. Said translinear amplifiers then control the switching transistors **Sw 1** to **Sw n**, which in turn switch on the individual small capacitors **Cap 1** to **Cap n** in the proposed steady ramp-up/ramp-down manner. The combination of one translinear amplifier **Tr.Amp k**, combined with adequate control circuit and one switching device **Sw k** could be considered as an individual capacitor switching stage, where one of said capacitor switching stages connects to one capacitor **Cap k** out of a set of small capacitors. Each of said capacitor switching stages is controlled through the common input **Vtune** and an individual input **Ref-in k**. All of these stages k = 1 to n have basically identical functional characteristics.

Please replace 7 paragraphs, starting with the original 1st paragraph at page 15 and up to the first full paragraph at page 18 with the following 7 amended paragraphs:

In the same way aAs described in said related patent application US Serial No. 10/764920, within a set of small capacitors **Cap 1** to **Cap n**, one capacitor after the other is switched in parallel to change the total capacity. Each capacitor has its individual switching device **Sw 1** to **Sw n.** To achieve a linear capacitance change, said capacitors are not switched on one by one in digital steps, however each capacitor is switched on partially in a sliding operation, starting at low value (0 % of its capacitance) and ending with the fully switched on capacitor (100 % of its capacitance). To achieve said sliding switch operation, a typical implementation uses FET- type transistors, one per capacitor. The switching operation of such FET-transistor can be divided into three phases: the fully-switched-off phase (the FET transistor's drain-source-resistance RDS is very high), a steady ramp-up/ramp-down phase or steady transition phase, where the series resistance of said FET-transistor linearly follows the gate voltage and steadily changes from high to low values or vice versa, and the fully-switched-on phase (~~the~~ said FET transistor's drain-source-resistance RDS is very low). **Fig. 10b** in US Patent Application Serial No. 10/764920, included by reference, visualizes the principal RDSon characteristic versus gate voltage of the switching devices **N1-5** of a single capacitor switching stage according to **Fig. 5** of the present application. By thoroughly controlling

such switching device within said steady ramp-up/ramp-down or steady transition area, the capacitor in series with said switching device is effectively switched in parallel to the other capacitors with a well-controlled proportion between 0 % and 100 %. "Steady" is meant in the mathematical sense of being free of jumps or breaks. The limits of said steady ramp-up/ramp-down or steady transition area is distinguished by the points, where a further change of the controlling signal of the switch does not lead to further decrease or increase of the series resistance of said switching device (except for a small, negligible change).

In case a specific member of said switching devices, as shown in **Fig. 6**, is switched fully-on, the parallel connection of the capacitor (in series with said switching device in view) is fully effective (i.e. is effective to 100 %). If however a specific item of said switching devices is switched fully-off, the parallel connection of the capacitor (in series with said switching device in view) is not effective at all (i.e. is effective to 0 %). While said switching device in view is operating within its steady ramp-up/ramp-down or steady transition phase, the capacitor may be effectively switched in parallel with any value between 0 % and 100 %. The effectiveness of the switching in parallel of said capacitor is well controlled through the translinear amplifiers **Tr.Amp 1** to **Tr.Amp n** and the relation of tuning and reference voltages, symbolized by the voltage dividing circuit of the resistor chain **R1** to **Rn**. One can assume the steady transition area of RDS changing to be, for example, between the 2 % point and the 98 % point and define these limits as the "desired steady transition area".

The terms "steady ramp-up/ramp-down phase", "steady transition" and "steady transition phase" or "steady transition area" ~~and "steady switching transition phase"~~ will be used throughout the document as synonyms, ~~to~~ defineing the phase of analog switching operation (i.e. steady ramp-up/ramp-down) as opposed to a pure digital switching operation (pure on/off). The area where said steady ramp-up/ramp-down is possible, is called the "steady ramp-up/ramp-down area" or "steady transition area". As said before, "steady" is meant in the mathematical sense of being virtually linear, free of jumps or breaks. In the same sense, the term "continual switching" means the ongoing process of "steady ramp-up/ramp-down switching". The term "area" in this context is used to express the "operating range" – the term "phase" is used to express the "operation in process" within said area.

Outside said "steady transition area" the switching device is not operating in a virtual linear mode any more, for example because it is reaching a switching transistor's saturation. The term "outside the steady transition area" therefore defines the capacitor switching stage's operating area outside its virtually linear "steady transition area". In **Fig. 7** the different operating areas are shown: the **Steady ramp-up/ramp-down Area**, the areas outside the steady transition area **Outside Lo** at the low (RDS) resistance side and **Outside Hi** at he high (RDS) resistance side. The cutoff edges are marked with **CutOff Lo** and **CutOff Hi**.

The switching device to switch on the capacitor, as used for the presented patent application, is a "switching device with a well controllable steady ~~transition~~ramp-

up/ramp-down ~~phase~~area "~~,~~; said device is in many cases shortly referenced ~~here~~in the instant document as "switching device".

A detailed view on the individual ramp-up functions at ~~the~~ each switching transistor's gate, of the circuit according to Fig. ~~3~~6, is shown in **Fig. 4a**. **Vg1** to **Vg7** are the gate voltage versus tuning voltage slope of the switching stages number 1 to 7 in this example. One can assume for example, ~~the~~ said switching transistor's steady ~~transition area~~change of resistance RDS between very high resistance and very low resistance ~~changing~~ to be effective~~, for example,~~ between the measured 2 % point and the 98 % point, i.e. the crossing with the 2 % line defines the start point of the steady ramp-up/ramp-down phase and the crossing with the 98 % line defines its end point~~ and define these limits as the "desired steady transition area"~~. All slopes of the individual gate voltages are strictly parallel. Threshold ~~points~~ levels **Th1** to **Th7** in **Fig. 4a** ~~are~~ may be equally spaced (distances **d1** to **d7** in **Fig. 4a**). **Fig. 4b** visualizes the overlapping switching operations of just 2 adjacent stages of the circuit according to **Fig. ~~3~~6**. **Overlap** is a measure, where **Vg2** just starts to switch on stage number 2 and where **Vg1** is still operating in the steady transition area (i.e. the RDS steady changing mode) for stage number 1. Because said gate voltage versus tuning voltage slopes are all in parallel, all overlaps are normally the same. Selecting the distance of the threshold ~~points~~ levels **Th1** to **Thn** (by properly designing the circuit to generate said threshold levels) also determines the amount of overlap between adjacent switching stages.

A translinear amplifier typically has a gain of 1. However, a gain different from 1 is also achievable, which, if implemented, gives one more degree of freedom in dimensioning the overlapping parameters: it allows to change the steepness of the gate control voltage change versus tuning voltage change. Now it is possible to select the switching overlap independent of the switching distance of adjacent capacitor switching stages. For example, the remaining overlapping of neighboring capacitor switching stages may be even further reduced, as the ~~slope~~ steepness of the steady ramp-up/ramp-down operation can be controlled with adequate selection of the gain. ~~See~~ **Fig 4c** demonstrates the reduced overlap of a steeper gate control voltage **Vg1s and Vg2s** of two adjacent capacitor switching stages, visualized as **Overlap Vg2s - Vg1s**~~ in Fig.~~ **4~~b~~**.

Please replace five paragraphs, starting at the last incomplete paragraph beginning at page 19 and up to the 1st full paragraph at page 22 with the following 15 amended paragraphs:
Note: in several places, the new text has only been moved to a new position.

There are various techniques for a circuit to generate a set of reference values and provide the threshold ~~points~~ levels to each of said ~~amplifier~~ capacitor switching stages. And there are various techniques for a circuit to provide a signal, dependent on the tuning voltage, dedicated for the voltage controlled capacitance change, to all of

said ~~amplifier~~ capacitor switching stages. As shown in Fig. 6 and Fig. 9, one solution for said circuit to generate a set of reference values is a simple resistor chain~~,~~. ~~and~~ A~~a~~ possible and minimal solution for ~~such~~ a circuit to provide the threshold ~~points~~ levels to each of said ~~amplifier~~ capacitor switching stages and for ~~such~~ a circuit to provide a signal, dependent on the tuning voltage~~,~~ and dedicated for the voltage controlled capacitance change, to all of said ~~amplifier~~ capacitor switching stages, is to connect said ~~reference points~~ individual threshold levels, ~~and~~ as well as said tuning voltage, with simple wire connections to the appropriate input lines of said translinear ~~inputs~~amplifiers.

Similarly, the output reference levels could be provided for example through a resistor network to provide individual output reference levels for each translinear amplifier (**Ref-out-1** to **Ref-out-n** in **Fig. 6**). Or, to provide the identical output reference level to all translinear amplifiers, a single signal could be connected to all inputs **Ref-out-1** to **Ref-out-n** of all translinear amplifiers (as indicated in **Fig. 6**).

Another key point of the invention is the implementation of signal ~~limiting~~ cutoff functions at both ends of the steady ~~switching transition~~ramp-up/ramp-down area. As long as the switching transistor is kept within its natural steady transition phase (RDS steady changing mode) the resistance of the transistor linearly follows the input difference of said translinear amplifier. Once the signal controlling the switching device leaves the desired steady transition area, the signal condition is now changed abrupt by one of the signal ~~limiting~~ cutoff circuits. **Fig. 7** visualizes this effect. The purpose is to overdrive said switching device to a fully-on state, when said switching device ~~is~~ operates outside its desired steady transition area on the lowe~~r~~ resistance side and to overdrive said switching device to a fully-off status, when said switching device ~~is beyond~~ leaves its steady transition area on the highe~~r~~ resistance side.

Fig. 7 of the instant document visualizes the idea of sharply cutting off said signal controlling the switching device as soon as a changing **Gate Control Voltage Vg** leaves the desired steady transition area **Steady ramp-up/ramp-down Area** at the cutoff edges **CutOff Lo** and **CutOff Hi**. For example, at the two desired points, beyond the 98 % on-point, said signal **Vg** controlling the switching device is rised sharply and below the 2 % on-point said signal **Vg** controlling the switching device is driven to rapidly switch-off.

Additional circuit elements, implementing said signal ~~limiting~~ cutoff functions, drive said switching transistor either into deep saturation (RDSon going to 0) or drive it into its extreme off state (RDSoff going very high) as soon as said switching device falls outside said desired steady ~~transition~~ ramp-up/ramp-down area.

A possible solution for said signal cutoff functions could be to implement said signal cutoff functions as separate circuits in combination with, but external to said translinear amplifier.

The principal concept of said separate circuits for said signal cutoff functions is shown in **Fig. 10a.** Switching devices **N3-10** and **N4-10** symbolize two circuits to drive said switching device to a fully on or fully off state, when said switching device operates outside said steady ramp-up/ramp-down area on the said switching device's low resistance side or high resistance side. The two control signals to either force said fully on or fully off state are **CtlCutOff Lo** and **CtlCutOff Hi**.

Another possible solution could be to implement said ~~Such~~ signal~~-limiting~~ cutoff functions~~ could, according to the invention, be implemented~~ within said translinear amplifier circuit~~,~~. ~~as it~~ Such solution integrated into the translinear amplifier is ~~shown~~ presented in ~~**Fig. 7** of~~ Patent Application US Serial No. 10/676919, filed Oct. 1, 2003, ~~and~~ which is hereby incorporated by reference. The relevant additional signal~~-limiting~~ cutoff function is presented there on page 6, 3^{rd} and 4^{th} paragraph, on page 14, 1^{st} and 2^{nd} paragraph, page 15 2^{nd} full paragraph and in **Fig. 7** with the additional circuits **ADD-COMP 1-7** and **ADD-COMP 2**. Circuit **ADD-COMP 2** in the referenced companion application is a real implementation of circuit element **N4-10** in **Fig. 10a** of the instant application and circuit **ADD-COMP 1-7** in the referenced companion application provides the control signal defined as **CtlCutOff Lo** in the instant application. The referenced application describes the implementation of the signal cutoff functions as cited in the following paragraph:

According to said second aspect, two additional circuit functions sharply limit the analog operating region through an extra current limiting transistor on one side and the purposely use of the voltage limited by the power supply on the other side. Key objective is to linearly control said translinear amplifier's output, for example for switching on or off a transistor in an application like it is shown in **Fig.** 4 (of the referenced application), and getting sharp cutoff edges, for example for switching on or off a transistor in said application to achieve minimum RDSon and maximum of RDSoff at the extreme ends. The desired output characteristic is visualized in **Fig. 5** (of the referenced application).

In **Fig. 5** of the referenced application and described there on page 15, 2^{nd} full paragraph, the linear operating region on line **50b** is marked as the area **59**. Once either output **Vout-p** or **Vout-n** reaches the cutoff voltage **Vlim** at point **59a** or when it reaches the power supply line **Vdd** at point **59b**, the linear operation is sharply cut off.

The above cited linear operating region marked as the area **59**, is the same as the steady ramp-up/ramp-down area of the instant application.

The specific implementation of the signal cutoff function integrated within said translinear amplifier of the referenced application takes advantage of the fact, that the output signal can completely swing up to the power supply rail, driving the Gate-Source Voltage of the switching device to zero, thus forcing a PMOS switch to go into high impedance state without any further measures. In the case the output signal could not swing up to the power supply rail or if a different type of switching device is used, an additional circuit similar in function to the circuits **ADD-COMP 1-7** and **ADD-COMP 2**

would be implemented. ~~Said signal limiting functions could however be implemented as separate circuits external to said translinear amplifier as well.~~

~~**Fig. 7** of the instant document visualizes the idea of sharply cutting off said signal controlling the switching device as soon as a changing **Gate Control Voltage Vg-7** leaves the desired steady transition area **Steady Transition Area** at the cut-off edges **CutOff Lo** and **CutOff Hi**. For example, at the two desired points, beyond the 98 % on-point, said signal **Vg-7** controlling the switching device rises sharply and below the 2 % on-point said signal **Vg-7** controlling the switching device is driven to rapidly switch-off.~~ **Fig. 8** presents the same behavior as Fig. 7 for a larger number of said capacitor switching stages. **Th1** to **Thn** are the selected threshold ~~points~~ for said switching to occur. **d1** to **dn** are the distances of said threshold ~~points~~, that normally are dimensioned to equal distance. The capactitor tuning voltage **Tuning Voltage Vctl** is supplied to all capacitor switching stages as a common signal.

Fig. 9 shows a realistic circuit diagram of an implementation, in accordance with an embodiment of this invention. **Tr.Amp 1** to **Tr.Amp n** are said translinear amplifiers, **Sw 1** to **Sw n** are the switching devices and **Cap 1** to **Cap n** are said capacitors that will be switched in parallel, resulting in the total capacitance **varCap**. **R1** to **Rn** build the resistor chain to produce references voltages for the amplifier of each stage, as already shown in Fig. 6. Similar to **Fig. 7**, the combination of one translinear amplifier **Tr.Amp k**, combined with adequate control circuit and one switching device **Sw k** could be considered as an individual capacitor switching stage, where one of said capacitor switching stages connects to one capacitor **Cap k** out of a set of small capacitors. Each of said capacitor switching stages is controlled through the common input **Vtune** and an individual input **Ref-in k**. In the implementation shown in **Fig. 9**, the output reference points **Ref-out k** of Fig. 6 are all connected to a common Reference point **Vref**. All of these stages k = 1 to n have basically identical functional characteristics

Furthermore, a concept of this disclosure is to compensate the temperature deviation, caused by the temperature characteristics of the switching device; **Fig. 10** presents this concept. One method is to use a device **N2-10** of the identical type of the switching device **N1-10** to produce a temperature dependent signal and feed it as compensating voltage **Vref-10** into the output reference point **Voutn-10** of the translinear amplifier. This will mirror the exact equivalent of the temperature error into the switching control signal **Vg-10** and compensate its temperature error. The output reference point **Voutn-10** in **Fig. 10** is the same point as the reference points **Ref-out 1** to **Ref-out n** in **Fig. 6**.

Please replace two paragraphs, starting at the 1st and 2nd paragraph beginning at page 23 with the following two amended paragraphs:

Typically, it would be desirable to achieve a linear relation between the tuning voltage and the capacitor variation, i.e. in a strictly linear mode. Then the reference voltages to compare with the tuning voltage would normally be equally spaced. However, to achieve a steady, but predefined non-linear relation instead, other reference voltage steps for said threshold ~~points~~ levels could also be selected, like spacing along a parabolic curve. As explained before, one circuit example is said resistor chain **R1** to **Rn**, or a similar circuit, to produce a series of voltage references **Ref 1** to **Ref n**, where each of said translinear amplifiers compares the tuning voltage with its dedicated reference voltage. To achieve a non-linear relation between ~~reference points~~ threshold levels and tuning voltage, a set of reference voltages will be provided, that are, instead of being equally spaced, spaced along a desired non-linear curve. As one suggested embodiment, such non-linear relation can be achieved by appropriate selection of the values of said resistor chain **R1** to **Rn.** Similar, the tuning voltage could be split into a multiple of tuning signals to feed them to the translinear amplifier inputs. Depending on the technique to implement the reference values defining said threshold ~~points~~ levels for each of the translinear amplifiers within ~~a~~ said *chain of said* ~~translinear amplifiers~~ capacitor switching stages, specific nonlinear relations of capacitance change versus tuning voltage can be constructed. The concept of said non-linear relation is demonstrated in **Fig. 12**, with **Curve A** and **Curve B** as examples.

In accordance with the objectives of this invention, a set of individual capacitors is implemented. Such capacitors could be metal or polymer capacitors, eventually mounted or fabricated on a common planar carrier or they could be integrated on a semiconductor substrate. The advantage of a capacitor not being of the junction (diode) type capacitor is the invariance due to voltage or temperature at the capacitor. The switching device is typically a FET transistor, which could be for example a P-~~MOS~~ channel or N-~~MOS~~ channel junction FET or a ~~C~~PMOS or NMOS FET. In the case complementary components are used all voltage levels would just be inverted without changing the principals of operation.